



Images

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT
COOPERATION TREATY (PCT)

(11) WO 97/36332

(13) A1

(21) PCT/IB97/00227

(22) 10 March 1997 (10.03.1997)

(25) English

(26) English

(30) 96200791.0

22 March 1996

EP

(22.03.1996)

(34) NL et al.

(43) 02 October 1997 (02.10.1997)

(51)⁶ H01L 29/788, 29/43, 21/8247, 21/336, 21/28

(54) FLOATING GATE NON-VOLATILE MEMORY DEVICE, AND A
METHOD OF MANUFACTURING THE DEVICE

(71) PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA
Eindhoven (NL).

(71) PHILIPS NORDEN AB [SE/SE]; Kottbygatan 7, Kista, S-164 85 Stockholm
(SE).

(72) DORMANS, Guido, Jozef, Maria; Prof. Holstlaan 6, NL-5656 AA Eindhoven
(NL). VERHAAR, Robertus, Dominicus, Joseph; Prof. Holstlaan 6, NL-5656
AA Eindhoven (NL). CUPPENS, Roger; Prof. Holstlaan 6, NL-5656 AA
Eindhoven (NL).

(74) HOUBIERS, Ernest, E., M., G.; Internationaal Octrooibureau B.V., P.O. Box
220, NL-5600 AE Eindhoven (NL).

(81) CN, JP, KR

(84) European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC,
NL, PT, SE)

(57) The invention relates in particular, though not exclusively, to an integrated circuit with an embedded non-volatile memory with floating gate (10). According to the invention, at least two poly layers of equal or at least substantially equal thickness are used for this device. The first poly layer, poly A, is for the floating gate (10) and for the gates (22) of NMOS and PMOS in the logic portion of the circuit. The second poly layer, poly B, serves exclusively for the control electrode (21) above the floating gate. If so desired, a third poly layer may be deposited for both the control electrode and the logic gates, so that the thickness of these electrodes, and thus their resistances, are given desired values. Problems like overetching and bridging during saliciding are prevented in that the control electrode and the logic gates have the same thickness.



THIS PAGE BLANK (USPTO)